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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/656,582	09/06/2000	Gordon Taylor Davis	RAL9-2000-0080-US1	RAL9-2000-0080-US1 9845	
25299	7590 06/18/2003	•			
IBM CORPORATION PO BOX 12195 DEPT 9CCA, BLDG 002			EXAMINER		
			HOANG, PHUONG N		
RESEARCH	TRIANGLE PARK, NC	27709	ART UNIT PAPER NUMBER		
			2126	2	
			DATE MAILED: 06/18/2003		

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application N .	Applicant(s)	- 0				
	09/656,582	DAVIS ET AL.					
Office Action Summary	Examiner	Art Unit					
	Phuong N. Hoang	2126					
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, - Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a reply be ting within the statutory minimum of thirty (30) day will apply and will expire SIX (6) MONTHS from a cause the application to become ABANDONE	nely filed s will be considered timely. the mailing date of this communicati D (35 U.S.C. § 133).	ion.				
Status							
1) Responsive to communication(s) filed on <u>06 S</u>	<u>September 2000</u> .						
2a) This action is FINAL . 2b) ☐ Th	is action is non-final.						
Since this application is in condition for allowed closed in accordance with the practice under a sixty of Claims.			s is				
Disposition of Claims 4)⊠ Claim(s) <u>1 - 29</u> is/are pending in the applicatio	n						
4a) Of the above claim(s) is/are withdraw							
<u></u>	WITHOUT CONSIDERATION.						
5) Claim(s) is/are allowed. 6) Claim(s) <u>1 - 29</u> is/are rejected.							
7) Claim(s) is/are objected to.							
8) Claim(s) are subject to restriction and/or	r election requirement						
Application Papers	oloollon roquii ollollii						
9) The specification is objected to by the Examine	r.						
10)⊠ The drawing(s) filed on <u>06 September 2000</u> is/a	re: a)□ accepted or b)⊠ objected	to by the Examiner.					
Applicant may not request that any objection to the	e drawing(s) be held in abeyance. S	ee 37 CFR 1.85(a).					
11) The proposed drawing correction filed on	_is: a)□ approved b)□ disappro	oved by the Examiner.					
If approved, corrected drawings are required in reg	bly to this Office action.						
12) The oath or declaration is objected to by the Ex	aminer.						
Pri rity under 35 U.S.C. §§ 119 and 120							
13) Acknowledgment is made of a claim for foreign	priority under 35 U.S.C. § 119(a	ı)-(d) or (f).					
a) ☐ All b) ☐ Some * c) ☐ None of:							
 Certified copies of the priority documents 	s have been received.						
2. Certified copies of the priority documents	s have been received in Applicati	on No					
 3. Copies of the certified copies of the prior application from the International But * See the attached detailed Office action for a list 	reau (PCT Rule 17.2(a)).	_					
14) Acknowledgment is made of a claim for domestic	c priority under 35 U.S.C. § 119(e) (to a provisional applica	ition).				
 a) ☐ The translation of the foreign language pro 15)☐ Acknowledgment is made of a claim for domesting 							
Attachment(s)							
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)	5) Notice of Informal I	/ (PTO-413) Paper No(s) Patent Application (PTO-152)	.•				
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DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 44 of fig 1, 80, 82, 84, 86, 88, 90, 92, 96, 98, 100, 102 of fig 3, 450 of fig. 4, 509, 510, 511, 521,of fig. 5. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 - 3, 6 - 16, 18 - 20, 23 - 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung, US patent no. 5,404,469.

As to claim 9, Chung teaches a network processing system including an embedded processor complex for controlling the programmability of a network processor, the complex including a plurality of protocol processor units (PPU), each PPU containing:

at least one core language processor (processor 10, col. 2 lines, 30 - 50),

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each CLP having at least two threads (threads, col. 2 lines 30 – 32),

a plurality of coprocessors (plurality of function units, col. 2 lines 30 - 50) for executing specific tasks for the system.

Chung does not teach multiple coprocessor interfaces to access and share the resources of the coprocessors with each CLP.

It would have been obvious for one skilled in the art by the time of the invention to recognize that there must have interfaces between core processor and coprocessors for communication.

As to claim 10, Solomon as modified by Chung teaches coprocessor interfaces are dedicated to support the code threads (threads can run between core processor and coprocessors through interface).

As to claim 11, Chung teaches checksum coprocessor (integer unit, col. 2 lines 30 – 45), datastore coprocessor (load/store unit). Stringcopy coprocessor, counter processor are generic coprocessors executing specific tasks.

As to claim 12, 13, 14, Chung teaches the network processing system of claim 10 further including a FIFO buffer (each buffer contains two horizontal instruction words and each horizontal instruction word contains a section corresponding to each function unit, col. 4 lines 5 - 10) between each thread and at least one of the coprocessors.

As to claim 15, 16, Chung teaches the network processing system including specific operating instructions (instructions shown in the instruction buffers are scheduled by the compiler statically....selecting threads, col. 4 lines 11 – 20)

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executed by the threads of the CLPs which result in commands to control coprocessor operation, which commands flow through the interface between the CLPs and the coprocessors.

As to claim 1 and 18, see claim 9 above.

As to claim 2 and 19, see claim 10 above.

As to claim 3 and 20, see claim 11 above.

As to claim 6 – 8, 23 - 25, see claim 12 – 14 above.

As to claim 26, 27, see claim 15, 16 above.

As to claim 28, Chung teaches the method according to claim 27 wherein the execution is either direct or indirect (the instructions issued to the function unit in the third clock cycle. By the end of the third clock cycle, all the instructions from the threads are issued, col. 4 lines 10 - 60).

Claims 4, 5, 17, 21, 22, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung US patent no, in view of Bitar, US patent no. 5,928,322.

As to claim 17 and 29, Chung does not teach latency events.

Bitar teaches the network processing system according to claim 15 wherein the instructions enable the system to identify long latency events (latency, col. 4 lines 55 – 67) and short latency events (low-latency, col. 3 lines 59 – 60) according to the expected response time to access data in response to a particular coprocessor command, and to grant full control to another thread when execution of an active thread

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stalls due to a long latency event, or to grant temporary control to another thread when execution of an active thread stalls due to a short latency event.

It would have been obvious to apply the teaching of Bitar to Chung's system because latency events used to control timing for executing threads.

As to claim 4, 5, 21, 22, Bitar teaches in the operation according to claim 3 further including a coprocessor execution interface arbiter to determine the priority between multiple data threads (changes to the priority of one or more real-time threads is another event, col. 4 lines 5 - 20).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong N. Hoang whose telephone number is (703) 605-4239. The examiner can normally be reached on Monday - Friday 9:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (703)305-8498. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7239 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)746-7140.

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